REMARKS

This communication is responsive to Office Action of February 22, 2005, in which Examiner:(A) requested a more aptly descriptive title; (B) requested a new abstract; (C) requested a reference in the specification to the earlier filed application of which this application is a divisional; (D) requested in regard to Claim 11, identification of support in the specification for, 1 unique identifier uniquely identifying the IC, 2 non-unique network address, 3 unique network address; (E) requested in regard to Claims 29, identification of support in the specification for, 1 the integrated circuit, 2 the memory, 3 the processor, 4 the cache controller; (F) rejected Claims 11 and 28-44 under 35 USC 103a as being unpatentable over Gentry (USP 5,778,180) in view of Johnson (USP 5,764,896) .

Applicant has amended Claims 11 and 29, 31, 37, 39 to include limitations reasonably expected in light of the Examiner's rejections. Applicant has canceled Claims 40-44. Claims 11, 28-39 remain for Examination.

(A) AMENDMENT TO TITLE

The Examiner has requested a more aptly descriptive Title.

Applicant has amended the Title.

(B) AMENDMENT TO ABSTRACT

The Examiner has requested a new Abstract;

Applicant has amended the Abstract.

(C) DIVISIONAL OF PRIOR FILED APPLICATION

The Examiner requested a reference in the specification to the earlier filed application of which this application is a divisional.

In the Preliminary amendment filed with the instant application on October 18, 2001 the Applicant amended the Specification to include the claimed divisional status with respect to prior application 09/162,681 filed on September 29, 1998 and entitled "*INTEGRATED*

CIRCUIT AND METHOD FOR BRINGING AN INTEGRATED CIRCUIT TO EXECUTE INSTRUCTIONS" .

In a TPC with SPE Zarni Maung on August 18, 2005 Supervisory Patent Examiner Maung accessed the above referenced matter and verified that the priority claim was correctly made and assured the Applicant that he need merely bring the above discussed preliminary amendment to the Examiner's attention, by way of responding to and addressing this objection/request.

The Examiner will please make of record the Applicant's proper and timely filed priority Claim and the divisional status of this Application from parent Application 09/162,681 now U.S. Patent 6,356,942 Issued March 12, 2002.

(D) REQUESTS FOR SUPPORT IN THE SPECIFICATION CLAIM 11

The Examiner requested in regard to Claim 11, identification of support in the specification for, 1 unique identifier uniquely identifying the IC, 2 non-unique network address, 3 unique network address.

The Applicant's integrated circuit begins its 'life' on a network anonymously, i.e. without either a unique network address or operational capability defined in terms of the peripheral device of which it will form a processing part. (Specification at page 8, lines 4-10, lines 24-26) During this initialization phase communications between IC and a network server include packets the payload portions of which contain the unique identifier, e.g. a random number, generated by the IC and the address portion of which contains a non-unique group id or broadcast address for the IC. At the end of the initialization phase the integrated circuit acquires from the server both a unique network address and a peripheral device specific operational functionality e.g. executing processes associated with a printer, card reader and camera for example. (Specification at page 11, lines 13-21) The following sections of the specification offer further support as follows:

> *"In an embodiment of the invention, these packets may contain a source address which is a group address and* ***payload which contains a unique identifier generated by each of the chips*** *140A-D to enable the server to distinguish one packet from the other. This identifier is not a unique destination address as is required in prior peripheral devices. Instead* ***rather***

than configuring each of the multi-mode chips 140A-D in the factory with the unique network ID network, the unique network ID will be assigned in subsequent processes. In an embodiment of the invention, each of the chips generates a random number and puts that in the payload portion of the responsive packet sent to the server. In addition the responsive packet sent by each of the multi-mode chips may contain the chip ID and the device ID." (Specification at page 9, line 26 to page 10 at line 9)

"The server then using the same group ID as a destination address, sends packets....in an alternate embodiment of the invention the server could include as a destination address a broadcast address." (Specification at page 10, lines 24-27) (See also FIG. 4A ref. no. 304, FIG. 4B ref. no. 306, FIG. 4C reference numbers 304 showing non-unique Group ID used as non-unique network address of IC during initialization phase) "In the BIOS phase of operation shown in FIG. 1A, the server 102 sends out a packet 110 having as a destination address a generic group identifier. This packet will be processed by any and all of the multi-mode chips 140A-D shown in FIG. 1A. Provided only that each of those chips has in local memory 202 a group identifier 242 which corresponds to the group identifier in the packet.." (Specification at page 13, lines 20-21)

"Each of the multi-mode chips 140A-D on each of the peripheral devices picks up every group packet but only utilizes the OS and/or application code from the packet containing a random number matching the random number generated by the specific multi-mode chip. In this manner, each of the peripheral devices processes only its own unique packet even though they lack at this stage a unique network address." (Specification at page 11, lines 5-10)

"The next portion of the payload field 316C contains a unique network address 440 assigned by the server for the specific peripheral device which generated the random number. Peripheral addresses are global and centrally administered by the server to assure that each address is unique. This unique network address will be used by the peripheral device and multi-mode chip in subsequent network communications. Thus, in all further communications with the network, packets sent to the peripheral device will not be sent on a group basis but will instead be sent on a targeted basis because the destination address field 304 of the LAN packet will contain a unique network address." (Specification at page 17, lines 3-17)

In light of the above referenced paragraphs in the specification as well as corresponding portions of the drawings the Applicant respectfully submits that the above referenced phrases are in fact supported in the specification.

(E) REQUESTS FOR SUPPORT IN THE SPECIFICATION CLAIM 29

The Examiner requested in regard to Claim 29, identification of support in the specification for, 1 the integrated circuit, 2 the memory, 3 the processor, 4 the cache controller;

The Applicant's integrated circuit (See FIG. 2, ref. 140A) has two modes; initiating and working. In the initiating mode, in an embodiment of the invention, a volatile cache memory (See FIG. 2, ref. 250) is disabled allowing the cache memory to serve as a temporary buffer for download of the peripheral device operating system (See FIG. 2, ref. 254) to a non-volatile main memory (See FIG. 2, ref. 220) on the peripheral device (See FIG. 2, ref. 120A). In the working mode, a controller (See FIG. 2, ref. 248) for the cache memory is enabled allowing caching in the cache memory of copies of recently used sections of main memory (See FIG. 2, ref. 220) for access by the processor (See FIG. 2, ref. 200). The following sections of the specification offer further support as follows:

> *"In the context of the invention, an integrated circuit (IC) denotes an electronic circuit in one piece, having conductors and components integrated therewith, i.e., a chip .... "(Specification at page 4, lines 6-8) "FIG. 2 is a hardware block diagram of the multi-mode chip 140A and a peripheral device 120A (see FIGS. 1A-D). The multi-mode chip 140A includes a central processing unit (CPU) 200, a local memory 202, a cache 204, a direct memory access (DMA) controller 206, a memory controller 208, address and data buffers 210A-B and an optional switch 212. The cache includes a cache controller 248 and a cache memory 250. " (Specification at page 11,lines 22-27) "An additional feature of the kernel BIOS is that it is capable of disabling the cache controller 248 to allow the transitory use of cache as a normal volatile memory. In the normal mode, the cache subsystem of the chip will have the functionality of checking hit/miss, dirty bits, etc. " (Specification at page 13, lines 14-17)*
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> *"...[T]he storage and OS/application code 254 from the server is downloaded to the multi-mode chip and stored in cache memory 250. Utilizing the storage code the operational*

processes transfer the operating system to main memory. With the device thus configured the multi-mode chip serves as the central processing unit for the web camera executing processes 176A (see FIG. 1D). The cache reverts to its normal function of keeping copies of recently used sections of main memory 220 for access by the CPU 200." (Specification at page 14, lines 17-23) "In the event the determination is reached that the multi-mode chip is in the run-time mode, i.e. that control is passed to process 708. In process 708 the cache 204 is enabled to function as a cache with either for example any number of cache policies including 'write-through' or 'copy-back' for example. Control is then passed to process 710 in which the operating system 256 stored on main memory 220 of the peripheral device (see FIG. 2) is loaded from main memory into RAM 226 to begin operation of the peripheral device as a web camera." (Specification at page 21,lines 6-12) "In an embodiment of the invention, the CPU 200 serves as the processor for not only the network interface including medium access control (MAC) functions but also packet assembler and disassembler (PAD). In an alternate embodiment of the invention, the CPU 200 serves as the processor for the peripheral device, e.g. the web camera 120A. The CPU 200 would then implement various image processing algorithms. In an alternate embodiment of the invention, the CPU 200 serves both as a network interface processor including MAC and PAD functions and also as the processor for the peripheral device." (Specification at page 21, lines 16-23)

In light of the above referenced paragraphs in the specification as well as corresponding portions of the drawings the Applicant respectfully submits that the above referenced phrases are in fact supported in the specification.

(F) <u>Rejection of Claims 1 and 28-44, under 35 U.S.C. 103(a)</u>

The Examiner has rejected Claims 11 and 28-44 under 35 USC 103a as being unpatentable over Gentry (USP 5,778,180) in view of Johnson (USP 5,764,896) .

Examiner has cited the Gentry reference as teaching a *"a processor ... configured to couple to the network and the peripheral device... processor operable during an initialization mode to generate a unique identifier...and to download the operating system to the peripheral*

device ...thereby enabling a run-time mode for the peripheral device." (Office Action of 2-22-2005 at page 5). Applicant respectfully rejects each of the above referenced characterizations of the Gentry reference.

The Gentry reference is directed to an asynchronous transfer mode (ATM) network interface card (NIC) on a computer with DMA transfer of received data directly to one or more user processes on the computer, rather than indirectly through a buffer on the NIC. "*...NIC demultiplexes ...incoming packet ...directly to its final destination using the ...concept of targeted buffer rings.*" (Gentry Abstract). "*...[I]llustrates an exemplary computer system network incorporating a ATM ...NIC...which utilizes the method and apparatus for reducing data copying overhead of the present invention*". (Gentry at Col 4, lines 8-11) "*Since there are multiple VCI's coming into a host, there can be multiple targeted buffer rings and multiple user processes can receive their data with no copying.*" (Gentry at col 3, lines 56-59 Emphasis Added) "*...[C]hannels which are tied directly to user application...*"(Gentry at col 6, line 65 Emphasis Added)

The Gentry reference has no teaching on peripheral devices, let alone the enablement of peripheral devices. A computer is not a peripheral device. Network attached peripheral devices, include devices peripheral to a computer such as the printer, card reader, video camera shown in the Applicant's disclosure. The Gentry teaching is directed to run-time data copying processes between NICs and associated computers coupled to an ATM network. The Gentry computers already have their operating system and the Gentry NICs already have their IP addresses Nowhere is download and enablement of an operating system for the Gentry computer NIC combinations disclosed. Thus, setup initialization and enablement of a peripheral device which are the subject of the Applicant's claimed invention are not disclosed in the Gentry reference. Rather Gentry is concerned with transfer of data for one or more user applications. A user application is not an operating system.

The Johnson reference is similar to the Gentry reference is several respects. It discloses a NIC coupled to a computer with reduced latency between the NIC and the computer to which it is attached. Nowhere are peripheral devices or enablement of same disclosed.

The Applicant therefore respectfully submits that the Applicant's claimed invention is not obvious in view of either the Gentry or the Johnson reference since neither of those references disclose method or apparatus for enabling peripheral devices, let alone the

Applicant's claimed limitations with respect thereto. The Applicant therefore respectfully requests that the Examiner withdraw the rejections under this part.

CONCLUSION

In view of the above remarks; the amendment of Claims 11 and 29, 31, 37, 39; and the cancellation of Claims 40-44 Applicant respectfully submits that remaining Claims 11, 28-39 have been placed in condition for allowance and requests that they be allowed. Early notice as to the allowance of all remaining Claims is solicited.

The Commissioner is authorized to charge any and all additional fees which may be required, including petition fees and extension of time fees, to Deposit Account No. 50-1338 (Docket No. AXISP702D1).

Respectfully submitted,
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Date: August 22, 2005

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